Please amend claims 7 and 14 as follows:

7. (Amended) The memory device comprising:

a memory cell region comprised of a memory cell array comprising a plurality of memory cells arranged as a matrix, each of said memory cells comprising first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said floating gate with the interposition of an interpoly dielectric film, and

a peripheral circuit region having disposed therein a plurality of second MOS field effect transistors, each unitary transistor having a second well region formed in a semiconductor substrate, a second diffusion layer formed in said second well and designed to function as source and drain, and gate electrodes formed on said second well with the interposition of a gate insulating film,

wherein isolation between said plurality of second MOS field effect transistors is effected by a shallow groove isolation method, and at least one of said gate insulating films of said plurality of second MOS field effect transistors comprises a first insulating film deposited on the semiconductor substrate,

wherein the interpoly dielectric film comprises a second deposited insulating film which is substantially equal to said first insulating film in thickness,

wherein said first and second insulating films are a silicon oxide film,

wherein nitrogen is introduced into said silicon oxide film, and

wherein the nitrogen concentration in said second insulating film is higher than that in the first insulating film.

14. (Amended)The memory device comprising:

a memory cell region comprised of a memory cell array comprising a plurality of memory cells arranged as a matrix, each of said memory cells comprising

first MOS field effect transistors each having a first well region formed in a semiconductor substrate, a first diffusion layer formed in said first well region and designed to function as source and drain, a floating gate formed on said well with the interposition of a tunnel dielectric film, and a control gate formed above said well with the interposition of an interpoly dielectric film, and

a peripheral circuit region provided with second MOS field effect transistors each having a second well region formed in the semiconductor substrate, a second diffusion layer formed in said second well region and designed to function as source and drain, and first gate electrodes formed on said second well with the interposition of a first gate insulating film, and third MOS field effect transistors each having a third well region formed in the semiconductor substrate, a third diffusion layer formed in said third well region and designed to function as source and drain, and second gate electrodes formed on said third well with the interposition of a second gate insulating film which is greater than said first gate insulating film in thickness,

wherein isolation in said peripheral circuit region is effected by a shallow groove isolation method, and said second gate insulating film comprises a first insulating film deposited on the semiconductor substrate.

wherein each of the interpoly dielectric film and the first gate insulating film comprises a second deposited insulating film,

wherein both of the first and second insulating film are a silicon oxide film,

wherein nitrogen is introduced into the silicon oxide film, and

wherein the nitrogen concentration in the films is higher in the order of interpoly dielectric film, first gate insulating film and second gate insulating film.

In the Abstract:

Please amend and replace the abstract provided on a separate sheet herewith.